Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD AND APPARATUS FOR CONTROLLING COMMON-MODE OUTPUT VOLTAGE IN FULLY DIFFERENTIAL AMPLIFIERS]

BACKGROUND OF INVENTION

[0001] The present invention relates generally to amplifier circuits, and, more particularly, to a method and apparatus for controlling common-mode output voltage in fully differential amplifiers.

[0002] Differential signaling has been commonly used in audio, data transmission and telephone systems for many years because of its inherent resistance to external noise sources. More recently, differential signaling has become popular in high-speed data acquisition wherein, for example, differential amplifiers are used to drive inputs of analog to digital converters. In particular, a fully differential amplifier is a differential amplifier that, in addition to

differential inputs, also includes differential outputs (as opposed to a single-ended output of standard operational amplifier). For example, the input and output differential signals may be voltage signals centered about $(V_{CC}-V_{SS})/2$, within the range (V_{SS}, V_{CC}), wherein V_{SS} is a substrate voltage and V_{CC} is a power rail (or core) voltage. Such devices provide increased immunity to external common-mode noise, reduced even-order harmonics, and twice the output swing for a given voltage limit as compared to single-ended systems.

[0003] With a fully differential amplifier, a common-mode feedback loop is used to set the common-mode voltage at the output of the amplifier. One technique for achieving this is to add auxiliary current sources to the active load in the differential amplifier and to control the gates/bases of the auxiliary sources with a feedback loop that adjusts the voltage on the gates/bases until the common-mode voltage at the output of the amplifier matches a reference input to the feedback loop. This in turn results in the use of additional current source devices that increase area and capacitive loading on the output nodes of the fully differential amplifier.

[0004] Accordingly, it would be desirable to be able to implement

a means for controlling the common-mode voltage in a fully differential amplifier structure without utilizing auxiliary current sources in the common-mode feedback loop, thereby saving device real estate.

SUMMARY OF INVENTION

[0005] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for controlling the common-mode output voltage in a fully differential amplifier. In an exemplary embodiment, the method includes comparing a sensed common-mode output voltage of the fully differential amplifier to a reference voltage, and generating an error signal representing the difference between the sensed common-mode output voltage and the reference voltage. The error signal is utilized to control the body voltage of one or more FET devices included within the fully differential amplifier until the sensed common-mode output voltage is in agreement with said reference voltage.

[0006] In another embodiment, an apparatus for controlling the common-mode output voltage in a fully differential amplifier includes a sensing scheme for determining a sensed common-mode output voltage of the fully differential amplifier. An error amplifier compares the sensed

common-mode output voltage to a reference voltage, the error amplifier configured to generate an error signal representing the difference between the sensed common-mode output voltage and the reference voltage. The error signal is coupled to a body terminal of one or more FET devices included within the fully differential amplifier so as to control the body voltage thereof until the sensed common-mode output voltage is in agreement with the reference voltage.

[0007] In still another embodiment, a method for controlling the common-mode output voltage in a fully differential amplifier includes comparing a sensed common-mode output voltage of the fully differential amplifier to a desired common-mode output voltage, and generating an error signal representing the difference between the sensed common-mode output voltage and the reference voltage. The error signal is utilized as an input to a coarse feedback loop, the coarse feedback loop coupled to a reference current mirror in the fully differential amplifier. The error signal is further utilized as an input to a fine feedback loop, the fine feedback loop configured to control the body voltage of one or more FET devices included within the reference current mirror until the sensed com-

mon-mode output voltage is in agreement with the desired common-mode output voltage.

[0008] In still another embodiment, an apparatus for controlling the common-mode output voltage in a fully differential amplifier includes a sensing scheme for determining a sensed common-mode output voltage of the fully differential amplifier. An error amplifier compares the sensed common-mode output voltage to a reference voltage, the error amplifier configured to generate an error signal representing the difference between the sensed common-mode output voltage and the reference voltage. The error signal is utilized as an input to a coarse feedback loop, the coarse feedback loop coupled to a reference current mirror in the fully differential amplifier. The error signal is further utilized as an input to a fine feedback loop, the fine feedback loop configured to control the body voltage of one or more FET devices included within the reference current mirror until the sensed common-mode output voltage is in agreement with the desired common-mode output voltage.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

[0010] Figure 1 is a schematic diagram of an existing fully differential amplifier, featuring the use of auxiliary current sources in the error feedback loop;

[0011] Figure 2 is a schematic diagram of fully differential amplifier, utilizing feedback control of the body voltage of devices already present therein, accordance with an embodiment of the invention;

[0012] Figure 3 is a schematic diagram of an alternative embodiment of the fully differential amplifier of Figure 2;

[0013] Figure 4 is a schematic diagram of an alternative embodiment of the fully differential amplifier of Figures 2-3; and

[0014] Figure 5 is a schematic diagram of still another alternative embodiment of the fully differential amplifier of Figures 2-4.

DETAILED DESCRIPTION

[0015] Disclosed herein is a method and apparatus for controlling common-mode voltage in fully differential amplifiers, without the use of auxiliary current sources in the (fine) error feedback loop. Briefly stated, in the present invention embodiments, the common-mode output voltage of a fully differential amplifier is controlled by modulating the body voltage of devices already present in the amplifier, as opposed to adding more devices (i.e., current sources)

for the specific purpose of common-mode control. It is assumed that in a triple-well bulk or SOI CMOS technology, for example, access to the body terminals of both N-type and P-type devices is available. Alternatively, at least one embodiment is shown in which only the P-type device bodies are controlled/adjusted. It should also be appreciated that such an embodiment would also be applicable to a traditional N-well CMOS technology.

[0016] Referring initially to Figure 1, there is shown a schematic diagram of a conventionally controlled fully differential amplifier 100. As is shown, the amplifier 100 includes a reference current source 102, and current mirror devices (NFETs) M6, M2, M5 and (PFETs) M7, M4, M3, M8 and M9. The differential input terminals IN_P, IN_M of amplifier 100 are coupled to the gates of NFETs M0 and M1, respectively, while the differential output terminals OUT_M, OUT_P of amplifier 100 are coupled to the drain terminals of M0 and M1, respectively. In order to determine the output common-mode voltage of the amplifier 100, a common-mode sensing network 104 (e.g., a resistive divider including resistors R0 and R1) is connected differentially across the output terminals. This configuration develops the common-mode voltage at the center tap point of the

two equally valued resistors. However, other common-mode sensing schemes as known in the art may also be used.

[0017] In any case, the sensed common-mode output voltage is coupled to the inverting terminal of a common-mode error operational amplifier 106, which compares the sensed common-mode voltage to a reference voltage (CM_TARGET) and drives a feedback path such that the common-mode output voltage is adjusted to match the reference voltage. In the conventional configuration of Figure 1, the output of error amplifier 106 is used to drive the gates of additional contributing PFET current source devices M8 and M9. The bulk of the PFET load conductance of the amplifier 100 is thus controlled in an open-loop manner by current mirror devices M4 and M3.

[0018] As indicated previously, the additional current source provided by the combination of M8 and M9 for open-loop control represents devices that increase the overall area of the amplifier, as well as adds to the capacitive loading on the output nodes of the amplifier. Therefore, in accordance with an embodiment of the invention, Figure 2 is a schematic diagram of a fully differential amplifier 200, in which the output of the common-mode error operational

amplifier 106 is used to adjust the body voltage of FET devices already included within the amplifier topology. In the specific embodiment illustrated, the output of the common-mode error operational amplifier 106 is connected to a pair of inverting amplifiers, NFETs M8 and M9, which in turn are coupled to the body terminals of load PFETs M4 and M3, respectively. Accordingly, depending on whether the sensed common-mode output voltage is above or below the reference voltage (CM_TARGET), the corresponding change in body potential of M4 and M3 will increase or decrease the voltage threshold thereof, thus altering the conductivity of M4 and M3 until the sensed common-mode voltage matches the reference voltage.

[0019] For example, if the sensed common-mode output voltage exceeds the reference voltage, the output of error amplifier 106 will increase the conductivity of M8 and M9, thus lowering the body potential of M4 and M3. This in turn increases the threshold voltage of those PFETs, rendering them less conductive and thereby causing the sensed common-mode voltage to decrease. Conversely, if the sensed common-mode output voltage is less than the reference voltage, the output of error amplifier 106 will decrease the conductivity of M8 and M9, thus raising the

body potential of M4 and M3. This in turn decreases the threshold voltage of the load PFETs, rendering them more conductive and thereby causing the sensed common-mode voltage to increase. In this embodiment, the maximum body potential for PFETs M3 and M4 is Vcc. This voltage is reached when M8 and M9 are turned completely off by the error amplifier. To ensure that the loop range is not restricted by this upper limit, the conductance respectively of M3 and M4 is nominally set relative to the conductance of M7 so that the body voltage required to balance the loop is always less than Vcc. This can be accomplished by making the widths of M3 and M4 slightly larger than the width of M7 so that the common-mode output voltage is always too high when M8 and M9 are off. This technique essentially adds a pre-bias or systematic common-mode offset to the loop.

[0020] As is also shown in Figure 2, a pair of load resistors R2, R3, is provided for inverting amplifiers M8 and M9. In addition, because the body voltages of M4 and M3 are adjustable, a clamping device is used to prevent the body-to-diffusion diodes present in M4 and M3 from being turned on. In the embodiment depicted, this function is implemented through a pair of clamping diodes D1, D0,

although any number of known clamping schemes could also be used. Furthermore, a frequency-compensating device is provided, as implemented in Figure 2 by capacitors C1, C0. The capacitors are used in order to set a dominant pole in the common-mode feedback loop to prevent it from oscillating spuriously. Again, more sophisticated frequency compensation methods as known in the art could also be used.

[0021] Figure 3 is a schematic diagram of a fully differential amplifier 300, in accordance with an alternative embodiment of the invention. As is with the case of the circuit of Figure 2, the output of the common-mode error operational amplifier 106 is also used to control FET body voltage. In this example, however, the body potential of PFET reference device M7 is coupled to the output of error amplifier instead of PFETs M4 and M3. This provides a simpler design, in that only a single clamping device D1 and frequency compensating device C1 need be added to the circuit. Moreover, since no NFET inverting amplifier devices are used in this embodiment, there is no need for additional load resistors associated therewith. Again, in this case the loop is pre-biased so that the range is not restricted. This can be accomplished in this embodiment by

increasing the size of M7 slightly with respect to M3 and M4.

[0022] Referring now to Figure 4, there is shown a schematic diagram of another fully differential amplifier 400, in accordance with an alternative embodiment of the invention. In this embodiment, the output of the common-mode error operational amplifier 106 is also used to control the body potential of the NFET bias current mirror device M2. This also provides a simpler design with respect to the embodiment of Figure 2, in that (again) only a single clamping device D1 and frequency compensating device C1 need be added to the circuit. Pre-bias of the loop in this embodiment is achieved by making M2 slightly larger.

[0023] Finally, Figure 5 is a schematic diagram of still another embodiment of a method and structure for controlling the common-mode output voltage of a fully differential amplifier. The fully differential amplifier 500 of Figure 5 provides a dual level of common-mode voltage control, through coarse/fine level adjustment, for enhancement of bi-directional adjustment (i.e., adjusting the common-mode output voltage in both positive and negative directions).

[0024] As is shown in Figure 5, a body reference voltage genera-

tor 502 is used to generate a suitable body voltage to be continuously applied to the amplifier PFETs M4 and M3 and selectively to M7. The body reference voltage may be chosen, for example, to be about halfway between the positive supply (V_{CC}) and the desired clamp level in order to prevent forward biasing of the body-diffusion junctions of the PFETs. In particular, the generation of this bias level in the body reference voltage generator 502 is accomplished by the resistor pair R2, R3 and buffer op-amp 504. The output of op-amp 504, configured as a voltage follower, sets the body voltage of M4 and M3 to the value defined by resistor pair R2, R3. It is also noted that the body reference voltage is also selectively applied to the body of PFET M7 whenever the amplifier 500 is in a first or "coarse" mode of operation.

[0025] Moreover, in the coarse mode of operation, the common-mode error operational amplifier 106 is disconnected from an analog feedback loop (similar to the feedback loop of Figure 3), and is instead used as a comparator in a digital feedback loop. More specifically, common-mode error operational amplifier 106 is used as a comparator to control the direction of a digital up/down counter 506 (or, alternatively, a more sophisticated successive approxima-

tion, averaging, or other calibration engine), thus resulting in an n-bit binary word at the output of the counter 506. It will be noted that the internal clock of up/down counter 506 is gated through the use of an AND gate 508 having by a coarse mode control signal and an external clock signal as inputs thereto. Thus, when the coarse mode is not asserted, the value of the counter 506 remains constant, independent of the state of the op amp/ comparator output.

[0026] The n-bit counter word generated by up/down counter 506 is coupled to a digital-to-analog converter (DAC) 510, the output of which contributes current along with current source M5 to the current mirror reference device M7 that biases the PFET loads in the main amplifier. It will be noted that the dimensions of the PFET mirror devices may be adjusted slightly so that the circuit is nominally balanced at the midpoint of the n-bit word count and the output range of the DAC 510.

[0027] Once a steady state condition with respect to the coarse calibration phase reached, the up/down counter value is nominally within 1/2 of a DAC least significant bit (LSB) of the count that is required at the DAC input to balance the circuit. At this point, the output of the counter 506 is held

at its present value, and the common-mode control loop is then switched over to a second or "fine" analog mode of operation. In this mode, the output of common-mode error operational amplifier 106 is used in an analog feedback loop to control the body of PFET M7 so that the common-mode target voltage is precisely achieved. In other words, the body of M7 is disconnected from the output of the body reference generator 502 and coupled to the output of the common-mode error operational amplifier 106.

[0028] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.